# Extensible FPGA Framework (EFW) For HiTech Global HTG-K7-PCIe Kintex-7 PCIE FPGA Module

### **Key Framework Features**

- Integrated, hardware verified solutions for 1G/10G Ethernet development
- HTG-K7-PCIe module targeted system building blocks of DMA Controllers, Ethernet MAC and PCS, PCIE application interface, AXI4 Interconnect, DDR3 and Flash Memory controllers
- Frameworks bundled with:
  - All Options: x8 PCIe Gen2 PCIe application interface, AXI4-Lite master/arbiter for memory mapped interface, Field Upgradeable (FUp) controller for in-system Flash programming and I2C controller
  - Ethernet Options: Synthesizable binaries and full simulation libraries GiGE, Low Latency 10G or Ultra-Low Latency 10G Ethernet solution
- Linux source code device drivers and APIs for PCIe interface and DMA controller
- Unified GUI (Binary) for the entire EFW with scripting support
- Lowest startup cost for developing complete 1G and 10G solutions with Kintex-7 FPGA
- Simplified, single-sourced licensing for all FPGA IP cores and drivers

# QUICKEST AND HIGHLY AFFORDABLE 1G AND 10G ETHERNET DEVELOPMENT WITH HTG-K7-PCIE MODULE

Extensible FPGA Framework (EFW) empowers FPGA developers with a verified set of productivity solutions, including module targeted physical interface components, device drivers and APIs for the HiTech Global HTG-K7-PCIE module.

Frameworks save months of development and debug time by enabling developers to skip the tedious and time-consuming phase of IP core integration, interface verification and firmware development.

| Framework Bundled Content                      | Framework Type |    |     | Required FMC |
|--|----------------|----|-----|--------------|
|  | Base           | 1G | 10G | Module       |
| Linux Device Drivers and APIs (Source)         | •              | •  | •   | -            |
| x8 Gen2 PCIe hard IP based PCIe Endpoint       | •              | •  | •   | -            |
| Wrapper (Verilog)                              |                |    |     |              |
| PCIe Thin Client for Memory Mapped Access      | •              | •  | •   | -            |
| (Netlist)                                      |                |    |     |              |
| AXI4-Lite Master and Arbiter with 32-bit       | •              | •  | •   | -            |
| control plane for registers accesses (Verilog) |                |    |     |              |
| 32-bit AXI4-Lite Slave for integrating user    | •              | •  | •   | -            |
| blocks (Verilog)                               |                |    |     |              |
| G18 Flash controller for in-system field       | •              | •  | •   | -            |
| upgrades (FuP) (Netlist)                       |                |    |     |              |
| I2C Controller (Netlist)                       | •              | •  | •   | -            |
| SPI Controller (Netlist)                       | •              | •  | •   | -            |
| Targeted, hardware verified DDR3 controllers   | •              | •  | •   | -            |
| with AXI4 wrapper (Verilog)                    |                |    |     |              |
| GiGE MAC with 1000Base-X Interface (Netlist)   |                | •  |     | FMC-X4SFP+   |
| Low and Ultra-Low Latency 10G Ethernet         |                |    | •   | FMC-X4SFP+   |
| option (Netlist) Latency optimized for         |                |    |     | FMC-SFP-OC   |
| financial market applications                  |                |    |     | FMC-X2QSFP+  |

\* GIGE and 10G UDP/IP Offload Engine (UOE) IP cores also available



#### Frameworks Take Care of the Rest Just Concentrate on "This" and "This"

## **Productivity Features**

**PCIe Bus Interface and Management:** Complete PCIe endpoint solution for the HTG-K7-PCIE with x8 Gen2 PCIe interface. Framework implements a 32-bit AXI4-Lite compliant register access interface for Non-DMA (single read/write) operations.

**Parameterized AXI4-Lite Inter-connect:** Complete, fully parameterized 32-bit AXI4-Lite inter-connect with Master, Arbiter and Slave in source (Verilog) code for register access.

**Ethernet Solutions for GiGE and 10Gbps:** HTG-K7-PCIE targeted and fully verified Ethernet interfaces using GiGE, Low Latency or Ultra-Low Latency 10Gbps Ethernet solutions. Exemplary Ethernet designs using Hitech Global HTG-FMC-X4SFP FMC module. Basic L2 packet generators and checkers (netlist) included for quick interface verification through GUI interface. GiGE and 10Gbps UDP/IP Offload Engine (UOE) IP cores also available for hardware protocol acceleration.

**BPI Flash Upgrade through PCIe:** Program and erase the parallel Flash memory on the HTG-K7-PCIE through the PCIe interface at very high speeds. Integrating the FUp controller allows any user design to be field upgradable through PCIe.

*I2C and SPI Controllers:* Flexible I2C and SPI controllers with AXI4-Lite host interface for peripheral device management.

Device Drivers: 64-bit Linux device drivers in source code for register access and interrupts.

APIs: C (source code) language function libraries and example test for register access and interrupts in source code.

GUI Interface: GUI application (Linux, Binary only) for control and configuration of all EFW components.



## Links to IP Core and Module Resources

- 10G Low Latency Ethernet IP: <u>http://www.hitechglobal.com/IPCores/10GigEMAC.htm</u>
- 10G Ultra-Low Latency Ethernet IP: <u>http://www.hitechglobal.com/IPCores/</u>

For more information: *Phone:* +1-408-781-8043 *Email:* info@hitechglobal.com



| Product Ordering Codes    |                      |
|---------------------------|----------------------|
| Base (No Ethernet/DMA):   | HTK-EFW-K7-PCIe-Base |
| GiGe Ethernet:            | HTK-EFW-K7-PCle-1G   |
| Low Latency 10G Ethernet: | HTK-EFW-K7-PCle-10G  |
| Ultra-Low Latency 10G:    | HTK-EFW-K7-PCIe-10GU |